a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the processor.

12. (Amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the processor.

23. (Amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

34. (New) The microcomputer according to claim 8, wherein the debug circuit includes the memory-mapped register.

35. (New) The microcomputer according to claim 19, wherein the debug circuit includes the memory-mapped register.

36. (New) The microcomputer according to claim 30, wherein the debug circuit includes the memory-mapped register.